Embedded Ceramic Resistors and Capacitors in PWB: Process and Performance

John Felten
Dupont I-Technologies
14 T.W. Alexander Drive
Research Triangle Park NC 27709
Tel: (919)-248-5688
Email:
John.J.Felten@usa.dupont.com

Richard Snogren
Coretec/SAS Circuits, Inc.
10570 Bradford Road
Littleton CO 80127
Tel: (303)-972-7826
Email:
richard@sascircuits.com

Jiming Zhou
Delphi Automotive Systems
1 Corporation Rd.
Kokomo IN 46904
Tel: (765)-451-9533
Email:
jiming.zhou@delphiauto.com

Summary:

Processing and performance of ceramic resistors fired onto copper foil and embedded into FR4 circuit boards are presented and discussed. Basic properties of ceramic capacitors fired on copper foil and similarly embedded are also presented and discussed. The performance of the resistors is similar to that of lanthanum boride based resistors processed on ceramic substrate—10 Ohms to 10,000 Ohms, with TCR's of ≤ (<=) 150 ppm/degree C. Resistive stability under thermal cycling and aging is excellent. Initial mechanical test data also appear (s) good, with excellent stability under flex testing of the FR4 board. The resistors can be laser trimmed with tolerance (3 sigma) of about 1.5 to 2 per cent achievable. Capacitors have k of 1000 to 2000, with breakdown voltage of about 800 volts at 25 microns. Capacitance density of 150 to 300 nanofarads per square inch is routinely achieved. Capacitor characteristic is X7R.

Ceramic bodies are weak in tension and strong in compression; the most important processing precaution is to avoid putting the resistors under tension during lamination. Performance after processing appears excellent by usual environmental tests; board tension encountered in actual use does not appear to be a problem. To date, five mil resistors appear too small to be screen printed with good CV and reliability. Ten mil and larger resistors are adequate in stability. Results of temperature stability, laser trimming and investigation of stress encountered in resistor terminations are presented and discussed.

Introduction

The high number of passives needed for high density IC chips, the resultant increasing circuit density of PWB's, and the trend to higher frequencies in the multi-gigaHertz range, are among the factors combining to increase pressure on passive components surface mounted on PWB's. Current practice with surface mounted chip passives is to migrate to smaller dimension chips, and combine passives in multi-element arrays. Use of 0201 or 01005 chips will become increasingly common over the next few years.

As operating frequencies continue to rise and package density increases, with some new chips having thousands) of decoupling capacitor plus resistor combinations, further adaptation will be needed. A recent NEMI roadmap[1] forecasts 40 per cent penetration of embedded passives into the PWB marketplace by 2008 in response to ongoing evolution of high frequency and high density semiconductor chips.

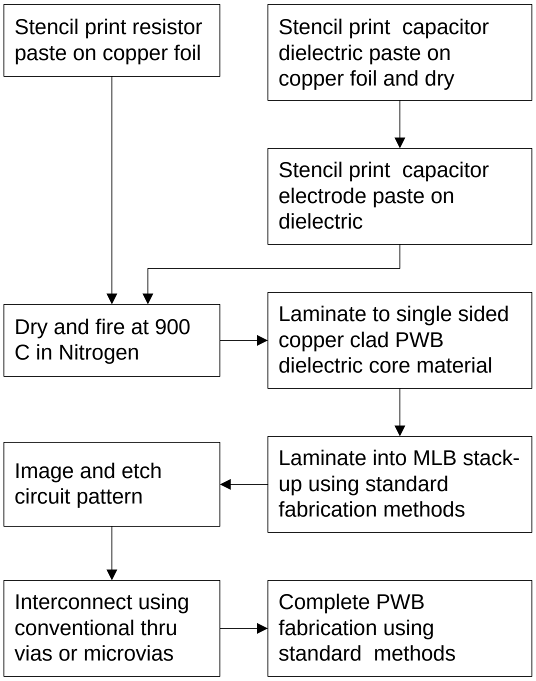
Several approaches[2] to embedding passives are now in use in the industry or under active development. The most frequently used material for embedded resistors is currently Ohmega-ply, a thin film laminate that is patterned using an etching process. Similarly, a thin plated material is under development by MacDermid. These materials have resistance of 50 to 250 Ohms/square. Polymer thick film resistors have been used for decades. Their relatively mediocre stability under high temperature/humidity has limited their use. Ormet is developing an organic/metal resistor system that that is curable at under 200 degrees C and has stability similar to that of polymer thick film compositions. DuPont also has a polyimide based polymer thick film resistor system.

Capacitive materials from several manufacturers are either available or under development as well. Organic and filled organic dielectric compositions are available from 3M, Sanmina, and Dupont. The Sanmina materials are commercially available to license by Sanmina, and the 3M and Dupont materials are under development. There are also thin film inorganic dielectrics that have very high capacitance, but also low breakdown voltage, because of their thinness. There is a fired ceramic dielectric under development by Dupont, which is covered in this report. This report also covers our development project with ceramic resistors fired onto copper foil, then laminated into boards after etching.

Why Ceramics

Reliability and proven history are the two primary drivers leading to the choice of thick film ceramics as embedded resistors and capacitors in PWB's. They are reliable because of the inherent stability of the inorganic materials used including their resistance to moisture, temperature, thermal shock, and electrostatic discharge. They have been in production in the ceramic passive component and ceramic hybrid industries for many years. Embedding these in PWB's involves merging two existing and time proven technologies; thick film processes and PWB multilayer processes.

Figure I: Process Flow for Embedded Passives



Process flow for embedded ceramic resistors and capacitors

On the thick film side of the equation, the commonplace formulation and manufacture of ceramic thick film paste materials (resistors, dielectrics and conductors) dates back to the early 1960's and is a mature production process today. The application of these materials to ceramic substrates using screen printing processes precisely controls the image features and material thickness. Firing in conveyerized nitrogen blanketed furnaces is a common mature production process today.

Using these methods to apply the ceramic materials to copper foil is the area where the PWB and thick film technologies merge. The control of this process has proven to be very manageable and not significantly unlike application to ceramic substrates.

On the PWB side of the equation, precisely reproducing conductor images in virtually unlimited geometries using standard photographic image transfer and chemical etching processes is a mature and proven process in volume production around the globe. Incorporating a variety of materials into the MLB composite, such as mixed dielectrics and a variety of dielectric and copper thicknesses, as well as interconnecting the conductor materials using conventional PTH vias and HDI microvias is also commonplace.

The merging of ceramic thick film and MLB technologies occurs when the copper foil carrying the ceramic components is laminated into a MLB structure and the component termination is formed using print-and-etch methods. These processes are so similar to conventional MLB lamination and imaging processes that they are easily controlled and managed. The process flow for the process of embedding ceramic passives into PWB's is shown in summary in Figure I.

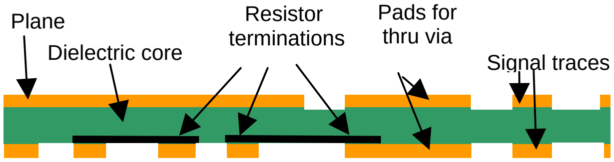
Ceramic Materials

The resistor materials are lanthanum boride based thick film resistor compositions which are being used in thick film circuits with copper conductors on alumina substrates. The differences with the embedded resistors are mainly in the processing, where steps must be taken to minimize tension on the resistors that occurs mainly during the lamination step to avoid cracking and delamination. This has necessitated the development of an adhesion promoting surface coating for the copper foil, and also a cured epoxy encapsulant applied before each lamination step with a twofold purpose: to reinforce the resistors during lamination, and to scatter laser light during laser trim. Without the encapsulant, laser damage to the PWB substrate would occur. The resistor compositions span four decades of resistance, from 10 Ohms to 10,000 Ohms per square. A 30,000 Ohm per square material is under development.

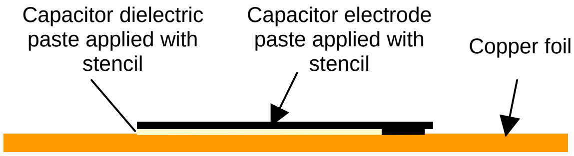
The ceramic dielectric material is also similar to other high K dielectric materials- doped barium titanate, with the distinction that this material is optimized for nitrogen firing, put into a modified organic vehicle to improve the burnout properties in inert atmosphere. The material also uses low level oxygen injection in the furnace burnout zone to improve burnout of organic matter.

Figure II: Resistor Process Stages

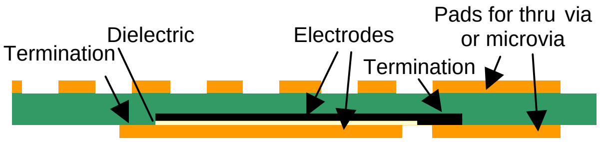
Ceramic Resistor Foil Fabrication (Printed and fired)



Ceramic Resistor Etched Core Fabrication (Laminated and etched)



Singulated or Discrete Ceramic Capacitor Foil Fabrication (Printed/fired dielectric and electrode)



Singulated or Discrete Ceramic Capacitor Core Fabrication (Laminated and etched)

Process Development-Resistors

Initial resistor prints on copper foil had poor adhesion, as evidenced by erratic resistance values, very poor tolerance of core flexure, and, in the case of higher Ohm resistors, separation from the foil after firing. This problem was solved by adding an adhesion promoting print to the copper foil before printing the resistors. The adhesion promoter is a copper/glass thick film ink that has good adhesion to the resistors as well as the foil. A second reason for the prefire before printing the capacitor prints is that the foil shrinks on the order of 0.3 mil per lineal inch of foil on the first firing; the foil has relatively much less dimensional change on subsequent firings.

The next problem causing erratic resistor performance was the wide terminations and runners that were used in test circuits for the resistors. Reducing the width of both terminations and runners to 10 mils or less greatly reduced the problem encountered with wide terminations. When scaling from initial 6”x6” substrates to 12”x18”, we also found that the steel plate used to planarize the foil with resistors during lamination was causing cracks in some of the resistors. Addition of an encapsulant before lamination, combined with use of a softer separator plate material, eliminates the cracks while providing a surface at the base of the copper that permits good etching of fine lines. The encapsulant also has an additive that permits laser trimming of the resistors without damaging the substrate. A second encapsulant print after laser trimming and before lamination of the core into the board also protects the resistors from lamination stress. The encapsulant-printed area around the resistors should be considerably larger in area than the resistors-plus-terminations for best results.

The critical process issues involved in converting the copper foil containing the resistors and/or capacitors into MLB innerlayer cores are:

1. Maintaining surface planarity so that the yields of subsequent print and etch process are not affected.
2. Using a stack-up of core, prepreg and padding materials that will minimize stresses on the embedded ceramic devices.
3. Scaling the images to maintain registration.

The process currently used, outlined above, produces a very high yield of stable resistors with dimensions of 10 mils width or greater. Resistors smaller than 10 mils width, and long serpentines, have poorer yields. Currently we plan to test yields and tolerances using stencil printing instead of screen printing. Better yields and tolerances of 5 and 10 mil resistors, and improved positional accuracy of printing are expected. Figure II shows the process steps employed in making an embedded ceramic resistor in a PWB.

Embedded Capacitors-Process

The process for embedded capacitors is similar to that for resistors. The adhesion promoting coating is printed and the foil is prefired with the coating. A second reason for the prefire before printing the capacitor prints is that the foil shrinks on the order of 0.3 mil per lineal inch of foil on the first firing, but has negligible dimensional change when subsequently fired. After the adhesion coat, two layers of dielectric are printed and fired, followed by a silver termination that is fired at low temperature (~250^{o} C). We are currently investigating materials with which both dielectric prints and a copper termination print are printed and cofired. Figure III is a cross section of a PWB containing embedded resistors and capacitors.

TABLE I: Thermal Stability of Resistors
B3H Coupon, Readings : Ohms (100 ohms)

100 Ohm Resistors- Average of 36 Resistors

Resistor Size	**Pre Bake**	**Solder 230^{0} Reflow**	**1000 Hrs. Therm. Cycle**
10 mil	141.5*	141.6*	141.7**
20 mil	107.2	110.4	110.4
40 mil	100.5	101.0	100.9
50 mil	96.4	97.1	96.6

* Two failed Resistor/36
** Three failed Resistors/36

10K Ohm Resistors- Average of 36 Resistors
Readings: Ohmsx1000

Resistor Size	**Pre Bake**	**230^{0} Solder Reflow**	**1000 Hrs. Thermal Cycle**
10 mil	26.1*	26.9*	26.4**
20 mil	14.1	14.1	14.3
40 mil	11.2	11.2	11.2
50 mil	10.4	10.4	10.4

* One failed Resistor/36
** Two failed Resistors/36

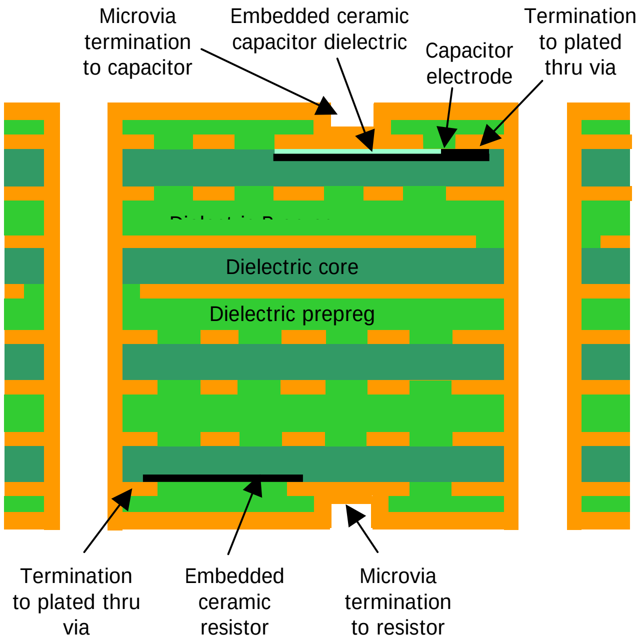
Table II: ESD Results-B3H Coupon, 100 Ohm
Avg. of 36 resistors, Readings : Ohms

Resistor Size	**2KV** *Pre/Post*	**4KV** *Pre/Post*	**6KV** *Pre/Post*	**8KV** *Pre/Post*
10 mil	135/135	132/131	134/131	130/133
20 mil	108/108	103/103	107/106	106/104
40 mil	89.6/92.1	90.5/90.5	86.5/86.4	92.8/92.2
50 mil	89.1/87.2	84.5/84.5	83.8/83.7	87.9/86.0

ESD Results-B3H Coupon, 10,000 Ohm
Avg. of 36 Resistors, Readings: Ohmsx1000

Resistor Size	**2 KV** *Pre/Post*	**4 KV** *Pre/Post*	**6 KV** *Pre/Post*	**8 KV** *Pre/Post*
10 mil	22.4/16.8	21.6/12.3	21.3/10.6	23.5/11.9
20 mil	12.9/10.7	11.5/8.8	12.4/8.4	12.1/7.5
40 mil	8.6/7.9	8.8/75.	9.2/7.5	9.2/7.2
50 mil	8.3/7.7	8.2/7.2	8.0/6.8	8.5/6.7

FIGURE III



Conventional and HDI MLB with Embedded Resistors and Capacitors, Terminated with Microvias and PTH

Laser Trim Results

Laser trimming of resistors through 1000 Ohms gives excellent results; the 10,000 Ohm material performance in initial tests is not as good. Further optimization of the process is currently being done, and we believe that we can get tolerances of +/-1.5% up to 1000 Ohms, and +/- 2 – 2.5% at 10,000 Ohms.

Performance-Resistors

The resistors perform very similarly to the same materials printed and fired on alumina substrates. The coefficient of variance, TCR, electrostatic discharge tests, and stability under thermal cycling are all similar to those of their analogs on alumina The resistors are currently encapsulated in an epoxy coating similar to FR-4 in composition, so high humidity test results are not as good as those of resistors on alumina with a ceramic encapsulant. Table I lists representative results of thermal stability tests. The electrostatic discharge tests are excellent with 100 Ohm resistors, and only fair with the 10,000 Ohm material (see Table II). The 10 Ohm and 1000 Ohm materials are not included in these test results; however, based on their performance on alumina they are expected to be excellent.

Future Challenges

It is noteworthy that the work accomplished to date has used only FR-4 laminates and 12 X 18 inch panels. Scaling the manufacturing panel size to the more common 18 X 24 inch panel is planned for the near future as well as evaluating other laminate materials. Other evaluations in progress include termination design, advanced precoating and encapsulating materials, interconnection design (through vias and microvias), resistors inline with conductors, resistor design (power vs. size), hermetic coatings for laminates, multiple values on a single layer, and, importantly, laser trimming.

Acknowledgements

The authors gratefully acknowledge the contributions Mr. Matt Snogren, of SAS, who carried out the fabrication of the finished resistor test boards. Dr. William Borland, of DuPont, developed the dielectric formulations and Mr. Saul Ferguson also of Dupont, carried out the actual fabrication of the printed and fired copper foils. Mr. Pierre Lamieux and Ms. Karen Walters of BTU Engineering, North Billerica, MA, allowed us to use their nitrogen furnace to fire foils. Jeff Simpson of Sierratherm, Watsonville, CA, also graciously arranged and assisted in the use of their facilities to fire foils. Kim Fjeldsted, of ESI, provided laser trim data with equipment under development at ESI. Dave McGregor, of DuPont PCM, provided invaluable consultation and collaboration in finalizing the design of test vehicles.

References

1. NEMI Roadmap for Passives, Year 2000
2. W.J. Borland and S. Ferguson, CircuiTree, March 2001

This NIST/AEPT Consortium work was performed partly under support of the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025.