Plated Embedded Resistors for High Speed Circuit Applications

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Embedded resistors are one of the enabling technologies for high frequency copper circuitry. A process has been developed to plate resistor elements exactly where required on inner layers. This means the circuit board fabrication shop can use a variety of laminate materials, can vary the resistivity from 25 to 100 ohms per square (based on plating time), and not inventory resistor foils as raw materials. Normal printed wiring board fabrication steps of activation and electroless plating are utilized to form the resistors. The process has been shown to make stable, easily laser trimmable resistor elements that are laminated inside multilayer printed circuit boards. The resistors show little change with multilayer pressing, little change with temperature change or exposure to moist atmospheres, and good stability with simulated circuit operation.

Introduction

One of the principles of electronics packaging is that each new product must be faster, lighter, and cheaper than the preceding generation. All of these may be addressed by embedding discrete components into the printed wiring board. The reasons for embedding include:

Faster – the linearity of signal into and out of embedded discrete components reduces the inductance of core-to-surface-return-to-core signal pathways. This reduced impedance allows higher frequency (faster) circuit boards. This is especially important considering the 1-10 gigahertz frequency now being used for tele-communications and signal routers. Also, surface area now taken by discrete components can by used to mount active devices closer.

Lighter – Embedding resistors and capacitors within circuit boards eliminates the solder connections of surface mount, and to some extent allows the circuit board materials to protect the device – lowering discrete component packaging. Also, since the embedded component is very near the desired signal termination for I/C's, copper circuitry to route to periphery is not needed. Discretes can be **under, not outside,** integrated circuits.

Cheaper – While this objective has yet to be proven, more savings in assembly costs are possible than the actual cost of the components themselves. This cost saving must be demonstrated through printed wiring board fabricators integrating new test and quality procedures (laser trimming) that are just being visualized.

Application – As most manufacturing processes for embedded passives utilize layers with exact values (e.g. ohms/square), the best applications of embedded passives are for assemblies that require large numbers of the same value discrete component. Examples of this include termination resistance and decoupling capacitance. Economic trade-off analyses of this effect have been sited by other authors (1). Most analyses can determine a crossover economic point where embedded discretes can cost less than surface mount. High speed digital, interface with fiber optics, and massive computation are indicated good applications for embedded discretes.

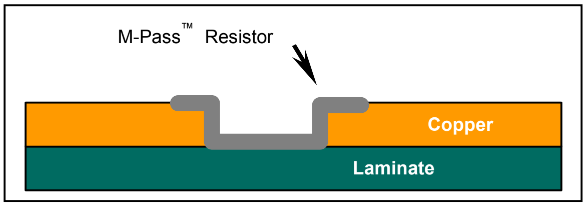
Process

One demonstrated successful resistor material uses electroplated nickel phosphorus as the embedded resistor element (2). This material is supplied as a coating on copper foil for inclusion on inner layers. Discrete values of resistivity are sold – 25 to 200 ohms per square, or more. The high resistance nickel/phosphorus layer is "under" all the copper circuitry of that board layer. It has been shown that nickel layers on circuit traces may cause signal loss at high frequency(3). For high speed, it is desirable to have resistor elements only where necessary on inner layers.

A modified electroless process using a nickel base (commercially designated M-Pass™ by MacDermid, Inc) allows selective deposition only in the desired areas on circuit board inner layers. This deposition is the result of traditional palladium catalyzation of dielectric surfaces, combined with the lithographic accuracy of dry film or liquid photoresists. Resistivity of the deposit is controlled by plating time – a longer

plating time creates a thicker (less resistive deposit).
Figure 1 shows a cross section diagram of this technology is shown below:

Figure 1



Process Steps
The fabrication process for the selective buried resistors is as follows in Figure 2

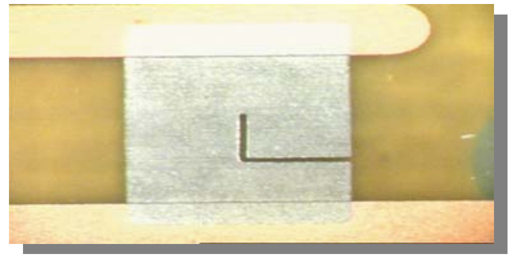
Figure 2 – Process Steps for Plated Embedded Resistor

Layer Preclean
Apply Layer Resist
Image
Develop/Etch/Strip
AOI
Clean/Condition Layers
Catalyze Surface
Apply Plating Resist
Image/Develop
Accelerate Exposed Catalyst
Plate Resistor Metal
Strip Resist
Laser Trim (if Required)
Coat Resistor Areas
Apply Oxide Alternative
Laminate Multilayer Board

The steps in red italics are an addition to the routinely used inner layer production process.

The only new operation in the above outlined process is laser trim. Technology is being developed by such companies as Electro Scientific Industries to accomplish this operation on printed wiring boards. Laser trimming is routinely used on the chip components mounted on the surface of boards today, but ceramic overcoats make this laser trim invisible to the human eye. A picture of a sample laser trim on embedded resistor material is shown in the next picture (Figure 3)

Figure 3 – Laser Trim –Courtesy of Electro Scientific Industries



Laser trim typically uses the "L" cut to first bring the resistor into gross tolerance, and then to finish the trim to a very close value. In this case, there was no damage to the underlying epoxy-glass substrate, since the plated resistor element is quite thin.

Table(1) below shows the values of resistance compiled for 12 boards, before and after laser trimming (Table 1.) Two plating times were used, both under the laser trimmed target of 50 ohms per square.

Table 1. Resistance Values Before and After Laser Trim

Summary of Measurement and Trim of Resistor Series

Board ID	Pre Trim Nominal (Ω)	Pre Trim +/−3σ(%)	Target (Ω)	Post Trim Average (Ω)	Post Trim +/−3σ(%)	Comments
#2 V(.050")	35.5	5.2	50.0	50.4	0.8	2.5 min. plate time
#2 W(.055")	34.5	8.4	50.0	50.3	0.3	
#2 X (.055")	34.1	11.4	50.0	50.0	0.2	
#2 EE(.040")	34.3	8.6	50.0	50.1	0.4	
#2 FF(.050")	32.9	4.0	50.0	50.0	0.3	
#4 T(.040")	28.9	13.7	50.0	50.1	0.4	
#4 U(.050")	31.0	7.5	50.0	50.0	0.3	
#4 BB(.030")	27.9	12.5	50.0	50.5	9.8	
AVERAGE	**32.4**	**8.9**		**50.2**	**1.6**	
#3 T(.040")	44.2	6.8	50.0	50.0	0.2	2.0 min. plate time
#3 BB(.030")	39.5	15.3	50.0	50.1	0.3	
#3 W(.055")	41.0	7.9	50.0	50.0	0.2	
#3 H(.040")	41.0	11.0	50.0	50.2	1.0	
AVERAGE	**41.4**	**10.2**		**50.1**	**0.4**	

Table 1 also shows that the 3 Sigma value of plated resistors may be quite satisfactory for some digital applications, without trim.

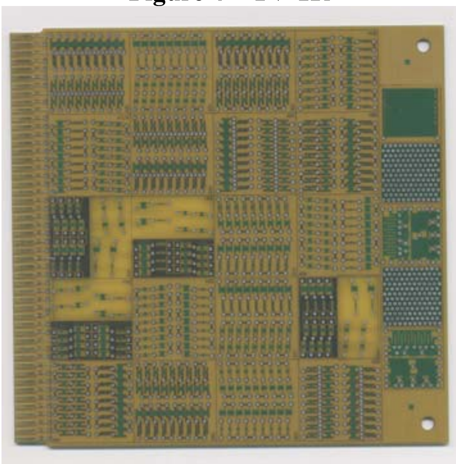
A new use for solder mask or screened dielectric material is the protection of the laser trimmed resistor through the oxide alternative step of conventional board manufacture. This protective layer maintains the "as trimmed" value very closely through subsequent handling and lamination. This is shown in Table 2 later in this paper.

Resistor Performance:

A current test of resistor performance involves participation in the NIST Advanced Embedded Passives Consortium. This program is performed under support of the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025. The project coordinator is the National Center for Manufacturing Sciences (NCMS). This program started in early 1999, and complete results will not be disclosed until the end of the project. However some preliminary comments can be made.

The first test vehicle built by the consortium consisted of a number of isolated and network resistors. This board is shown in Figure 4:

Figure 4 – TV-1R



This test vehicle has been designated public property and can be used by companies to prove in their resistor technology. The design files are available through the National Center for Manufacturing Sciences.

The target performances of candidate materials in the consortium is given in Table 2:

Table 2 – Desired Properties in Resistor Materials

Resistor Atribute	Baselin e SMT	Baseline Embedded	Progra m Target
Ω/square	Range	25-200	Range
Drift with Time	< 2%	< 2%	< 2%
Change - Frequency, Temp, Humidity	< 2%	< 2%	< 2%

In an accelerated test with 85% relative humidity and 85° C temperature, the resistor material passed. 1000 hours exposure.

Also, in a simulation of power up and turn off, the TV-1R Test Vehicles were cycled from -35° C to +125°C for 500 cycles. Again, the resistor material met the ± 2% specification.

Finally, the resistor values obtained in laser trimming the embedded components at inner layer fabrication, must be maintained through layer lamination and conversion into a final multilayer board.

The process for producing these layers was as follows:

- Expand and standardize the location of resistor terminations to facilitate "probe card" measurement of resistor values
- Expand the card size – Figure 4 TV1R to approximately 12 inches square.
- Terminate all resistors at an edge – using all four edges for contact points on 100 mil centers.
- Cover resistors with protective material, and use the conveyorized oxide replacement chemistry from production to treat layers after trim and before pressing.
- Use approximate 11x11 inch cap sheets for the of low flow prepreg for the lamination cycle – leaving the contact points available for measurement after pressing.

This procedure means that the outer layer need not be drilled, imaged, plated, and etched to isolate measurement points. Thus, the simulation inner layer core can be measured, trimmed to value, cap sheet laminated, and re-tested in a very short time – hours, instead of several days with the standard circuit board outer layer fabrication process. While the leads from the resistors will be longer than actual use, the change in resistance value will be solely due to the lamination step. Perhaps this process is less suitable for high frequency property testing., but it is quite useful for physical property change during fabrication.

Table 3 shows the values obtained in the simulation of multilayer fabrication.

Table 3. Plated Resistor Values Before and After Board Lamination

Summary of Lamination of Trimmed Resistor Series					
	Before Lamination		After Lamination		
Board ID	Average (Ω)	1s (Ω)	Average (Ω)	1s (Ω)	Average % Change (Ω)
#2 V (.050")	52.5	0.2	51.6	0.3	-1.75
#2 W (.055")	52.6	0.7	52.0	0.8	-1.19
#2 X (.055")	52.2	0.4	51.4	0.4	-1.59
#2 EE (.040")	51.7	0.4	51.0	0.7	-1.26
#2 FF (.050")	51.5	0.3	50.7	0.4	-1.61
#4 T (.040")	52.4	0.9	51.2	0.4	-2.13
#4 U (.050")	52.6	0.3	51.5	0.4	-2.04
#4 BB (.030")	53.1	1.8	51.7	1.8	-2.6
#3 T (.040")	52.8	0.9	51.4	0.6	-2.51
#3 BB (.030")	53.7	1.2	52.5	1.2	-2.36
#3 W (.055")	53.9	1.0	52.9	0.8	-1.84
#3 H (.040")	52.7	0.6	52.0	0.7	-1.27
AVERAGE	**52.6**	**0.7**	**51.6**	**0.7**	**-1.8**

Conclusions:

A selective application process has been demonstrated allowing embedded resistors to be formed only on the areas of inner layers where they are needed. This process allows fabrication of resistors entirely at the circuit fabrication shop – no purchase of special foils or laminates is required. The process of resistor formation uses conventional board processing steps.

Laser trim is easily accomplished on the plated resistors with no damage to the underlying dielectric substrate. Trimmed resistors are stable after trim and through layer lamination and outer layer circuit formation.

By successive imaging steps, it would be possible to form resistors of values from 25 to 100 ohms/square on the same layer.

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References:

(1) P. Sandborn, B. Etienne, and D. Becker, "Analysis of the Cost of Embedded Passives in Printed Circuit Boards" in *Proceedings of the IPC Annual Meeting and Technical Conference* (These proceedings), Orlando, FL, October 2001

(2) Patent 4,808,967 "Circuit Board Material", assigned to Ohmega Electronics

(3) D. Cullen, B. Kline, G. Moderhock, L. Gatewood, "Effects of Surface Finish on High Frequency Signal Loss Using Various Substrate Materials", Proceedings of the IPC Expo Conference, April, 2001.