

Advanced Embedded Passives Technology Consortium

Industry Seminar
January 30, 2003
Austin, TX



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Presentation of AEPT Project Results

Jan. 30, 2003 Agenda

Start 8:00 am

- **Welcome: AEPT Project**
 - Overview, Origin, Participants - Larry Marcanti, Nortel & Mike Schen, NIST (Tab 1)
- **AEPT Test Vehicles:** TV1, J. Zhou, Delphi (Tab 2) and TV2, R. Sheffield, Nortel (Tab 3)
- **OEM Emulators and lessons learned** - Nortel (Tab 4), Delphi (Tab 5), HP (Tab 6)

Break 10:00 – 10:15

- **Materials and Board Fabrication:** DuPont (Tab 7), Coretec (Tab 11)
3M (Tab 8), MacDermid (Tab 9), Merix (Tab 10)

Lunch 12:00 – 1:00

- **Component Trimming Session**
 - Laser Trimming, Values Upward, Kim Fjeldsted, ESI (Tab 12)
 - Inkjet Trimming and Rework, Values Downward, Virang Shah, MicroFab (Tab 13)
- **Modeling Session**
 - Overview of Cost Modeling Tool and Availability - C. Palesko, Foresight (Tab 14)
 - Cost Modeling - Peter Sandborn, Calce (Tab 16)
 - Neural Net Electrical Modeling - Dr QJ Zhang, Carlton University (Tab 15)
 - Question and Answer

Break 3:00 – 3:30

- **Infrastructure Going Forward**
 - IPC Standards and UL - Dave McGregor, DuPont (Tab 17)
 - Developing Infrastructure for Advanced Substrate Technology – Bob Pfahl, NEMI (Tab 18)
 - IPC and NWSC Crane - Embedded Passives Proposal - Ron Thompson, NWSC (Tab 19)
 - IPC Expo Special Activity - Dennis Fritz, MacDermid (Tab 20)
- **Embedded Passive Q/A Session**
 - OEMs, Fabricators, Material Suppliers, Support Teams
- **Summary / Key Lessons Learned** - L. Marcanti, Nortel

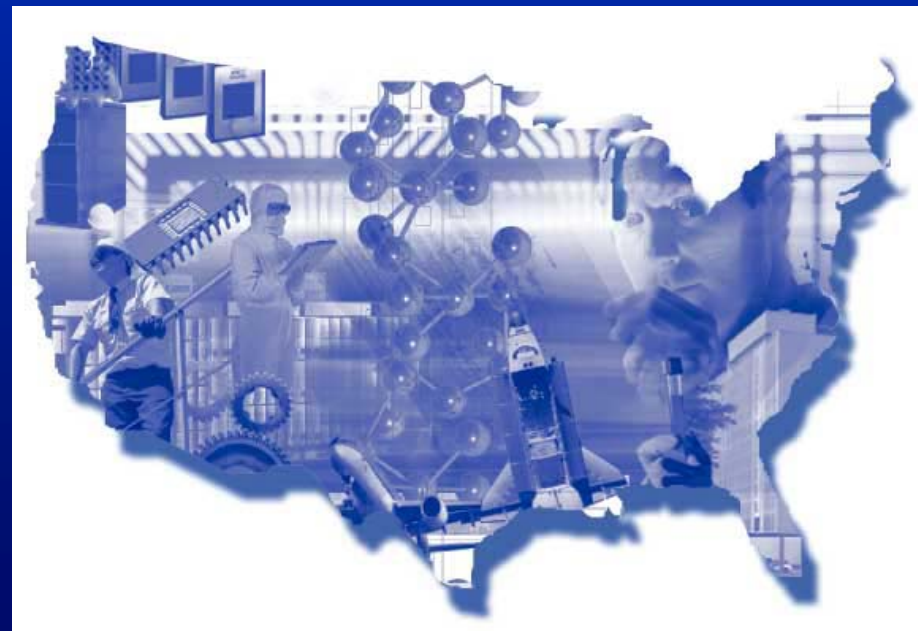
Adjourn 5:30

AEPT Program Team

- Material/Technology Suppliers
 - 3M - material
 - DuPont i-Technologies - material
 - MacDermid - material
 - MicroFab - ink jetting technology
 - ESI – measurement, trim & test technology
- Board Fabricators
 - Merix
 - Coretec
- Cost Modeling
 - Foresight Systems
- OEMs
 - Nortel Networks
 - Delphi Automotive Systems
 - HP
- Management / Industry Liaison
 - NIST
 - NCMS
 - IPC
 - NEMI
- Contractors
 - Neural Net Modeling
 - Carleton University

The Advanced Technology Program, ATP

To accelerate the development of innovative technologies for broad national benefit through partnerships with the private sector.



ATP is part of NIST



- ❑ \$820 million annual budget
- ❑ 3,000 employees
- ❑ 1,500 technical staff
- ❑ 1,600 guest researchers
- ❑ \$1.5 billion co-funding of industry R&D
- ❑ National measurement standards

Helping America Measure Up

ATP - Thirteen Years of Innovation

- Since 1990, 5,451 proposals submitted to 43 competitions, requesting \$11.7 B from ATP
- 642 projects awarded with 1,329 participants and an equal number of subcontractors
- 195 joint ventures and 447 single companies
- \$3.9 billion of high-risk research funded
 - ATP share = \$2.0 billion
 - Industry share = \$1.9 billion
- Small businesses are thriving
 - 63% of projects led by small businesses
- Over 160 universities participate
- Over 25 national laboratories participate

ATP - Advanced Embedded Passives

- Industry-led program
- Funded as part of ATP's 1998 *Microelectronics Manufacturing Infrastructure* program
- Four year, \$16.1 M effort
 - \$8.3 M industry
 - \$7.8 M government
- Involvement across the entire value chain
 - 12 companies
 - 3 Industry associations/consortia
 - 2 universities

The AEPT

To develop the materials, design, and processing technology for embedding passive devices into circuit board substrates to improve the cost, space requirements, performance, and reliability of circuit boards.

Objectives:

- Meet the needs of the microelectronics industry for compact, high performance products that incorporate proven EP technology.
- Provide usable, cost-effective solutions for large format circuit boards that demonstrate high manufacturing yield.
- Provide the cost modeling, performance simulation, and design tools that can be easily used by product designers.
- Reduce the system cost of resistors to half that of chip resistors.

Project Approach

Phase 1 - Screening Tests for Test Vehicle (TV-1)

- TV-1 proves feasibility of materials and fabrication.
 - Testing:
 - Temperature Coefficient of Resistivity (TCR)
 - 85/85 - 1000 hours unbiased
 - Thermal cycle -40° to +125°C - 500+ cycles
 - Liquid to liquid thermal shock -35°C to +125°C, 500 cycles
 - ESD test up to 8KV
 - Value after multiple cure cycles
 - Value after three reflow cycles
 - Current-carrying capacity - pulsed and constant
 - 60/90 with 48-volt bias -168 hr
 - Initial characterization for high-speed applications

Project Approach (continued)

Phase 2 - Electrical Performance

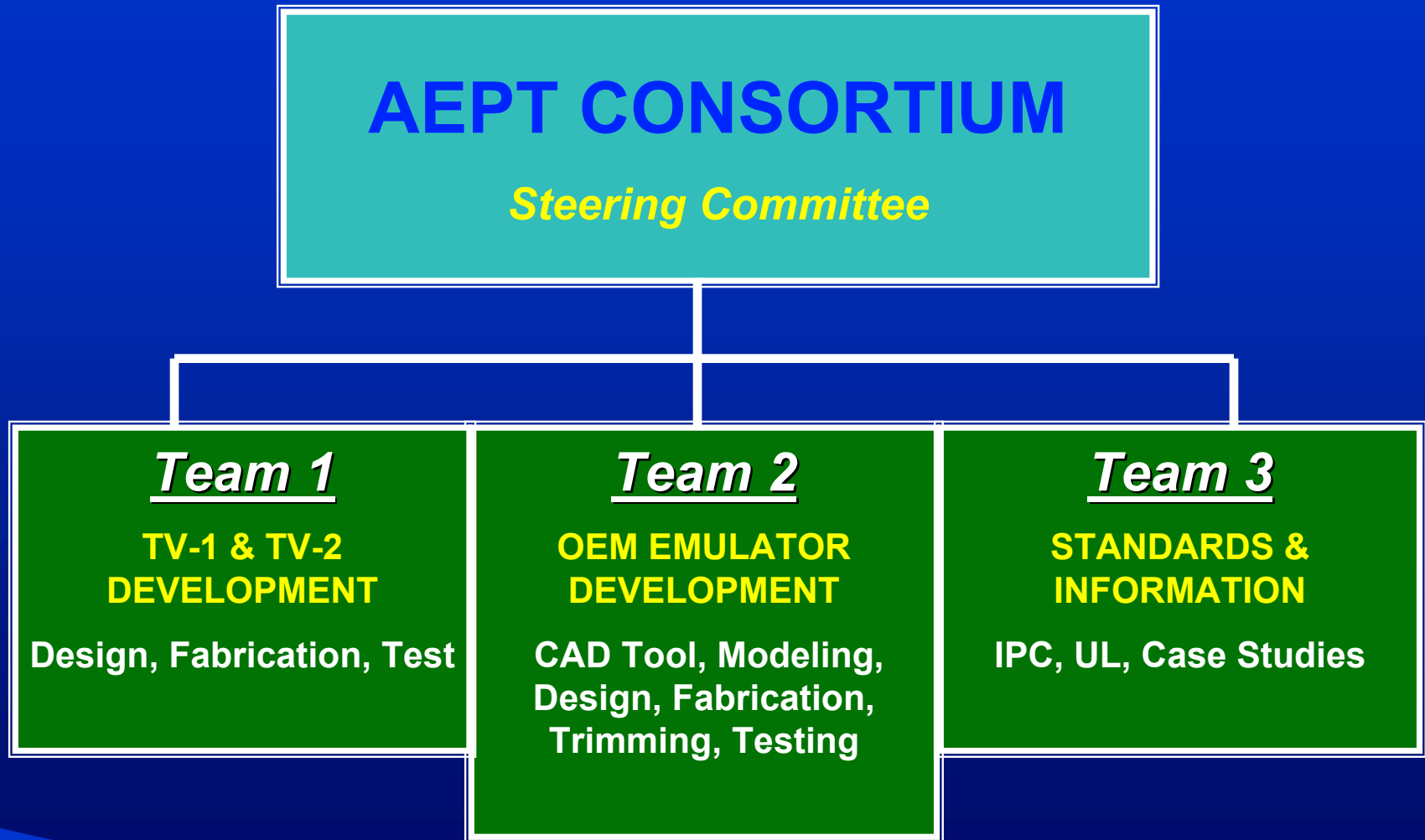
- High frequency (>5 GHz)
- Test vehicles (TV-2) designed to verify models by empirical measurement.
- Neural net technology applied to modeling results so that the computational overhead can be reduced and integrated easily into commercial computer-aided design (CAD) tools.
- Applications exclusively using embedded resistors or capacitors can exploit these results in high-speed designs.

Project Approach (continued)

Phase 3 - Resistors and Capacitors in Same Circuit Board

- Board fabrication processes modified to allow simultaneous implementation of both the resistors and capacitors.
- The cost model refined to reflect the dual resistor and capacitor processes.
- The performance simulation model and design rules refined throughout Phase 3.
- OEM emulator applications using both embedded resistors and capacitors take advantage of these results.

Project Structure



Key Accomplishments

- New resistor and capacitor materials solutions for the electronics industry's need for compact, high performance products that incorporate characterized technology.
- User-friendly cost modeling, performance simulation and design tools for product designers.
- Demonstrated manufacturing solutions for new materials.
- Demonstrated signal integrity improvements and design simulation tools at speeds higher than 2.5 GHz.
- Laser trim and test equipment that allows greater accuracy for embedded resistor technology.
- IPC and UL standards development well underway.
- Follow on work Crane labs & NEMI programs